WHAT IS CLAIMED IS:

1. A memory system comprising:

a memory device further comprising an array of cells formed in rows and columns;

a control signal controlling operation modes of the memory device; and a generator receiving the control signal providing a refresh request at a same period if the control signal is deactivated, providing no refresh request in response to a first state of the control signal if the control signal is activated, and providing a refresh request in response to a second state of the control signal if the control signal is activated.

- 2. The system of claim 1, the generator providing a refresh request at a same period in response to the second state of the control signal if the control signal is activated.
- 3. The system of claim 1, the generator providing refresh requests at different periods in response to the second state of the control signal is activated.
- 4. The system of claim 2, the control signal further comprising a pulse width smaller than half the same period.

- 5. The system of claim 1, the generator further comprising a clock generator generating a clock signal at a same period if the control signal is deactivated.
- 6. The system of claim 1 wherein the control signal is connected to a fixed voltage level when deactivated.
- 7. The system of claim 1 further comprising: a column decoder including a plurality of pass gates; and an amplifier unit disposed between the memory device and the column decoder further comprising a plurality of sense amplifiers corresponding to the pass gates.
- 8. The system of claim 1, the memory device being operated in continuous access cycles in response to the first state of the control signal.
- 9. The system of claim 1, the memory device being operated in continuous refresh cycles in response to the second state of the control signal.
- 10. A method of operating a memory device including an array of cells formed in rows and columns comprising:

providing a control signal;

activating the control signal, the activated control signal including a first state and a second state;

continuously performing access cycles in response to the first state of the activated control signal in one part of a period; and

continuously performing refresh cycles in response to the second state of the activated control signal in another part of the period.

- 11. The method of claim 10 further comprising providing the period within which each of the cells is refreshed before data stored therein are lost.
- 12. The method of claim 10 further comprising allocating to each of the access cycles a first access time for selecting and sensing a row of cells and a second access time for data output in continuously performing the access cycles.
- 13. The method of claim 10 further comprising allocating to a first of the access cycles a first access time for selecting and sensing a row of cells and a second access time for data output, and allocating to each of the remaining access cycles the second access time.
 - 14. The method of claim 10 further comprising: deactivating the control signal; and generating a refresh clock signal at a same period.

- 15. The method of claim 10 further comprising providing the control signal with a pulse width smaller than half the period divided by the number of total refresh cycles performed.
- 16. A method of operating a memory device including an array of cells formed in rows and columns comprising:

providing a control signal including a first state and a second state;

determining a period within which each of the cells is refreshed before data stored therein are lost;

determining the number of refresh cycles to perform in the period;

performing at least one refresh cycle in response to the second state of the control signal; and

allowing at least one access cycle to perform in response to the first state of the control signal.

- 17. The method of claim 16 further comprising continuously performing access cycles in one part of the period, and performing refresh cycles in another part of the period.
- 18. The method of claim 16 further comprising performing a refresh cycle at each of a plurality of sub-periods in the period.

- 19. The method of claim 18 further comprising performing a refresh cycle at each of the sub-periods of a same time length.
- 20. The method of claim 18 further comprising performing a refresh cycle at each of the sub-periods of different time lengths.
- 21. A method of operating a memory device including an array of cells formed in rows and columns comprising:

providing a control signal;

deactivating the control signal by connecting the control signal to a fixed level; providing a refresh request at a same period;

activating the control signal;

providing no refresh request in response to a first state of the activated control signal; and

providing at least one refresh request in response to a second state of the activated control signal.

22. The method of claim 21 further comprising:

determining a period within which each of the cells is refreshed before data stored therein are lost; and

determining the number of refresh cycles to perform in the period.

- 23. The method of claim 22 further comprising determining the same period as dividing the period by the number of refresh cycles to perform in the period.
 - 24. The method of claim 21 further comprising: maintaining the control signal at the second state; and continuously performing refresh cycles in the period.